REMARKS

Claims 8 and 22 are objected to by the Examiner because of various informalities. By this amendment, Claim 7 is cancelled without prejudice and Claim 8 has been amended to correct the identified typographical error. That is, as amended, Claim 8 now depends upon Claim 1. Therefore, the Applicants' respectfully submit that the § 112 rejection of Claim 8 should be withdrawn. Claims 1-14, 16, and 18-22 have also been amended without adding any new subject matter. Specifically, Claim 1, as amended, now incorporates subject matter of dependent Claim 7 and independent Claims 11 and 19 essentially each incorporate a similar subject matter.

The Examiner states that Claims 7 and 8 are not understood because the Specification and Drawings failed to disclose the claimed features therein. However, as noted above in the context of the amendments to Figures 3b, support for amended Claim 1 may be found in the Application's Specification on, for example, page 16, lines 4-7. In this manner, the semiconductor device of amended Claim 1 is patentably distinguishable over the art of record.

In the Office Action, Claims 1-6, 9-13, 16 and 18-22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Elenius (U.S. Patent No. 6,287,893). As the Examiner well knows, and anticipated reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. In re Bond, 15 U.S.P.Q. 2d 1566, 1567 (Fed. Cir. 1990). Applying this legal standard, it is respectfully submitted that Claims 1-6, 9-13, 16 and 18-22 are not anticipated by the Elenius reference.

Pursuant to the present amendment, independent Claim 1 has been amended to recite a second solder bump formed over a second absorption layer, wherein the first absorption layer and the second absorption layer are laterally isolated from each other by a spacing of approximately 1-100μm. It is respectfully submitted that this feature of separating adjacent solder bumps on adjacent first and second absorption layers by a narrow spacing of 1-100 μm, as defined by amended independent Claim 1, is not disclosed or suggested in the Elenius reference.

In general, the Elenius reference is understood to be directed to simultaneously forming solder bump pads as well as metal redistribution traces that electrically couple such solder bump pads with the conductive bond pads of the underlying integrated circuit. See Abstract, Figure 2, Col. 6, lines 31-37 and lines 56-63. According to the Elenius reference, openings are typically provided in wafer passivation layer above conductive bond pads 18/20 to allow access thereto. In addition, patterned openings are provided within the first passivation layer 24 above each of the conductive pads 18/20 and at those locations at which solder bump pads will ultimately be formed. An Under Bump Metallurgy (UBM) layer is provided on the surface semiconductor wafer 14, providing a solder bump pad 26 or an UBM interface 26 that is in direct contact with the solder ball 28. See Col. 7, lines 12-13 and lines 30-35 and lines 42-46.

However, the UBM layer in Elenius is not disposed between a contact pad and a solder bump as is the first absorption layer in amended Claim 1. Moreover, spacings, let alone narrow spacings between adjacent solder bumps formed on the adjacent absorption layers, as shown in Figure 3b, is nowhere disclosed or suggested in the Elenius reference. Instead, because of the openings provided in the wafer passivation layer 24 above the conductive bond pads 18/20 and at

those locations at which solder bump pads are formed, alpha particles from the solder bumps or from the environment may enter sensitive regions of a semiconductor device via these openings, wires and bump pads, respectfully. This radiation may cause malfunctions of sensitive circuit elements. These openings may further constrain the design of a semiconductor device, leading to a more complex design process and a reduced efficiency of the resulting device.

As thus understood, it is respectfully submitted that the Elenius reference does not anticipate the pending claims for many reasons. Fundamentally, the present invention is directed to providing adjacent absorption layers separated by narrow spacings such that most of the surface of the semiconductor device is covered by the absorption layers. These adjacent absorption layers substantially absorb alpha particles impinging on the semiconductor device, providing spacing between adjacent solder bumps formed on adjacent absorption layers, and ensuring electrical isolation between the solder bumps. See, for example, Specification on page 16, lines 4-7. At least this fundamental concept is nowhere disclosed or suggested in the Elenius reference. Thus, for at least this reason, it is respectfully submitted that all anticipation rejections of Claim 1 in view of the Elenius reference, and all claims dependent therefrom should be withdrawn. Similarly independent claims 11 and 19 have been amended in a manner similar to that set forth with respect to claim 1. Therefore, for at least reasons set forth above in the context to Claim 1, it is respectfully submitted that the Elenius reference does not anticipate independent claims 11 and 19, as well as claims depending therefrom, respectfully.

Claims 1-5, and 9-17 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Chiu (U.S. Patent Application No. 2003/0119300). Applicants respectfully

traverse the Examiner's rejection. The Examiner cites Figure 1d and paragraphs 0061 and 0063 of Chiu, for teaching the features in Claims 1 and 2. It is respectfully submitted that the methodology defined by independent claim 1, as amended, is not disclosed or suggested in the Chiu reference. Pursuant to the amendments and arguments set forth herein, reconsideration of the rejection of Claims 1-5 and 9-17 in view of the Chiu reference is respectfully requested.

Generally, the Chiu reference is understood to be directed to a method of making a bump on a substrate using an under bump metallurgy deposited over an upper passivation layer and the content pad. The Chiu reference does not disclose or suggest forming absorption layers such that the thickness of the absorption layers is configured to stop alpha particles of at least 5.4 MeV. Moreover, Chiu does not disclose providing spacing between adjacent solder bumps that are formed on the adjacent absorption layers, thereby insuring electrical isolation between the solder bumps. The method of forming a bump on a substrate of the Chiu reference involves providing openings in photoresist layers down to the under bump metallurgy such that the openings are aligned with the contact pad. See page 3, paragraph 0021.

Through these openings, however, alpha particles from the solder bumps or from the environment may enter sensitive regions of the semiconductor device in the Chiu reference, causing problems induced by alpha particles emitted from the solder bumps. Without spacing between the absorption layers, the adjacent solder bumps may not be isolated from each other either. In fact, none of the cited reference seems to consider the problem of soft error in a semiconductor device due to the emission of alpha particles from the solder bumps. That is, absorption of the alpha particles with energy of about 5.4 MeV, may cause soft error in the

semiconductor device suggested by the Chiu reference. Accordingly, it is respectfully submitted that the Chiu reference does not anticipate Claim 1, as amended. The amendments and arguments concerning amended Claim 1 also hold for independent claim 11 and claims depending therefrom.

In view of the foregoing, Applicants respectfully submit that all pending claims are in condition for immediate allowance. The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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